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SPECIFICATION

METAL-TO-METAL ANTIFUSE STRUCTURE AND FABRICATION METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to antifuse technology. More specifically, the present invention relates to metal-to-metal antifuse structures and fabrication methods.

2. The Prior Art

Antifuse devices are known in the art. Antifuse devices comprise a pair of conductive electrodes separated by at least one layer of antifuse material and may include one or more diffusion barrier layers. Prior to programming, antifuses exhibit very high resistance between the two electrodes and may be considered to

be open circuits. A programming process disrupts the antifuse material and creates a low-impedance connection between the two conductive electrodes.

Antifuses are generally classifiable in two categories. A first type of antifuse has a doped region in a semiconductor substrate as its lower electrode and a layer of metal or doped polysilicon as its upper electrode. The antifuse material typically comprises one or more layers of silicon nitride or silicon dioxide. This type of antifuse is referred to as a substrate antifuse.

A second type of antifuse has a first metal layer disposed above and insulated from a semiconductor substrate as its lower electrode and a second metal layer as its upper electrode. The antifuse material typically comprises a layer of a material such as amorphous silicon and may be accompanied by one or more barrier metal layers separating it from lower and upper metal interconnect layers. This type of antifuse is referred to as a metal-to-metal antifuse.

Numerous structures for metal-to-metal antifuses have been proposed for and are known in the art. Illustrative and non-exhaustive examples of metal-to-metal antifuses are shown in United States Patent No. 5,272,101 to Forouhi et al.

BRIEF DESCRIPTION OF THE INVENTION

A metal-to-metal antifuse according to the present invention is compatible with a Cu dual damascene process and is formed over a first Cu metal layer planarized with the top surface of a lower insulating layer. A lower barrier layer is disposed over the Cu metal layer. An antifuse material layer is disposed over the lower barrier layer. An upper barrier layer is disposed over the antifuse material layer. An upper insulating layer is disposed over the upper barrier layer. A second Cu metal layer is planarized with the top surface of the upper insulating layer and extends therethrough to make electrical contact with the upper barrier layer.

A method for fabricating a metal-to-metal antifuse according to the present invention comprises forming a lower barrier layer over a lower Cu metal layer planarized with the top surface of a lower insulating layer. An antifuse material

layer is then formed over the lower barrier layer. An upper barrier layer is formed over the antifuse material layer and the upper barrier layer and antifuse layer are defined. An upper insulating layer is formed over the upper barrier layer and antifuse layer and a via is formed to expose the top surface of the upper barrier layer. A second Cu metal layer is formed and planarized with the top surface of the upper insulating layer and extends therethrough in the via to make electrical contact with the upper barrier layer.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

FIG. 1 is a cross-sectional view of a metal-to-metal antifuse according to the present invention.

FIGS. 2A through 2D are cross-sectional views of the metal-to-metal antifuse of FIG. 1 taken after completion of selected steps in the fabrication process in order to illustrate the method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

Referring first to FIG. 1, a cross-sectional view shows a metal-to-metal antifuse according to the present invention. The metal-to-metal antifuse according to the present invention is compatible with a Cu dual damascene process and will be disclosed herein in the environment of an integrated circuit employing such a process for metalization. To illustrate how the antifuse of the present invention fits in an integrated circuit process employing a Cu dual damascene metalization process, metal-to-metal antifuse 10 is shown disposed next to a contact structure 12 disposed between two Cu metal layers in the integrated circuit.

Two different portions 14 and 16 of the lower Cu metal layer are shown disposed in lower insulating layer 18. Portion 14 of the lower Cu metal layer is associated with antifuse 10 and portion 16 of the lower Cu metal layer is interconnect metal. The vias containing portions 14 and 16 of the lower Cu metal

layer are shown including lining layers 20 as is known in the Cu metalization art. In addition, both portions 14 and 16 of the lower Cu metal layer are shown including contacts (reference numerals 22 and 24, respectively) for making electrical connections to circuit elements or metal layers (not shown) disposed beneath lower insulating layer 18. The thin SiN layer 26 shown surrounding portions 14 and 16 of the lower Cu metal layer is an artifact of the damascene process as is known in the art.

A cap layer 28, which may comprise SiN or a similar capping material, is disposed over the portions 14 and 16 of the lower Cu metal layer and the thin SiN layer 26. Regions 30 and 32 comprising a layer of TaN are disposed in vias in the cap layer 28. Region 30 is a lower barrier metal layer for antifuse 10. A layer of antifuse material 34, which may comprise, for example, a layer of amorphous silicon, is disposed over the lower barrier metal layer 30 and an upper barrier metal layer. An upper barrier metal layer 36 is disposed over the layer of antifuse material 34. A cap layer 38 is disposed over the upper barrier metal layer.

An upper insulating layer 40 is disposed over the cap layer 38. As presently preferred, insulating layer 40 may comprise a lower portion formed from fluorosilicate glass (FSG) and an upper portion formed from TEOS. Two different contact portions 42 and 44 of an upper Cu metal layer are shown disposed in upper insulating layer 40. Contact 42 of the lower Cu metal layer is associated with antifuse 10 and contact 44 of the lower Cu metal layer is associated with interconnect metal. The vias containing contact portions 42 and 44 of the upper Cu metal layer are shown including lining layers 20 as is known in the Cu metalization art.

Referring now to FIGS. 2A through 2D, a method is illustrated for fabricating a metal-to-metal antifuse according to the present invention. Because the elements illustrated in FIGS. 2A through 2D in many instances correspond to elements depicted in FIG. 1, elements in FIGS. 2A through 2D corresponding to elements in FIG. 1 will be designated using the same reference numerals as used in FIG. 1.

Referring first to FIG. 2A, a portion of the metal interconnect structure of the integrated circuit is shown after processing has progressed to the point where a lower insulating layer 18 has been deposited using conventional semiconductor processing techniques and lower Cu metal interconnect layer including portions 14 and 16 has been formed therein along with contacts 22 and 24 for making electrical connections to circuit elements or metal layers (not shown) disposed beneath lower insulating layer 18. The vias containing portions 14 and 16 of the lower Cu metal layer are shown including lining layers 20 as is known in the Cu metalization art. The top surfaces of the lower Cu metal interconnect layer and the lower insulating layer 18 have been planarized as is known in the Cu damascene metalization art. A thin SiN layer 26 surrounds portions 14 and 16 of the lower Cu metal layer and is an artifact of the damascene process as is known to persons of ordinary skill in the art.

As shown in FIG. 1, a first cap layer 28 formed from a material such as SiN, SiC, or another etch-stop layer with a low dielectric constant, having a thickness in the range of from about 10nm to about 200 nm has been deposited over the portions 14 and 16 of the lower Cu metal interconnect layer and the lower

insulating layer 18 using conventional deposition techniques. Conventional masking and etching steps (not shown) are used to form vias in the first cap layer 28 to expose the top surfaces of portions 14 and 16 of the lower Cu metal interconnect layer, after which the masking layer is removed using conventional mask-stripping steps.

A lower barrier metal layer, comprising for example, a layer of TaN or TiN, having a thickness in the range of from about 10 nm to about 200 nm has been blanket deposited over the existing surface. Known CMP techniques are then used to remove the lower barrier metal in regions other than in the vias in the first cap layer. FIG. 2A shows the structure existing after performance of the lower barrier metal CMP step.

Referring now to FIG. 2B, a layer of antifuse material 34, which may comprise, for example, a layer of amorphous silicon having a thickness in the range of from about 10 nm to about 70 nm, is blanket deposited over the lower barrier metal layer 30. A non-exhaustive list of other antifuse materials suitable for use in the present invention includes SiN/α-Si, SiN/α-Si, SiN/α-Si/oxide, SiC,

and α-C. Persons of ordinary skill in the art will understand that the antifuse programming voltage (VBG) exhibited for antifuses fabricated according to the present invention will depend on the composition and density of the antifuse material used as well as its thickness.

An upper barrier metal layer 36 comprising for example, a layer of TiN or TaN, having a thickness in the range of from about 10 nm to about 200 nm has been blanket deposited over the layer of antifuse material 34 using conventional deposition techniques. Next a masking layer 50 is applied and the stack including the antifuse material layer 34 and the upper barrier layer 36 is defined using conventional etching technology. FIG. 2B shows the structure remaining after the defining etch step but prior to removal of masking layer 50.

Referring now to FIG. 2C, after definition of the antifuse material layer 34 and the upper barrier layer 36, a second cap layer 38, formed from a material such as SiN, SiC, or other etch-stop layer having a low dielectric constant, having a thickness in the range of from about 10 nm to about 200 nm is blanket deposited over the exposed surface using conventional deposition techniques.

Next, an upper insulating layer 40 is deposited over the second cap layer 38. As presently preferred, insulating layer 40 may comprise a lower layer 54 formed from HDP fluorosilicate glass (FSG) and an upper layer 56 formed from TEOS. First, the FSG layer is formed to a thickness of between about 300 nm and about 400 nm using conventional high-density plasma techniques. Next, the TEOS layer is formed using conventional TEOS deposition techniques. The TEOS layer 56 is then planarized using CMP techniques. FIG. 2C shows the structure remaining after the CMP planarization process step.

Referring now to FIG. 2D, a masking layer 58 is applied over the top of TEOS layer 56 and and vias are formed in the second cap layer 38 in preparation for depositing the upper Cu metal layer 58 including contact regions 42 and 44 and to expose the top surfaces of the upper barrier metal layer 36 and the TaN region 32 over region 16 of the lower Cu metal layer. FIG. 2D shows the structure remaining after formation of the upper Cu metal layer (including liners 20) but prior to definition of contact regions 42 and 44 therein as a part of the damascene process.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.